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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,217	08/22/2001	Brent Keeth	DB000575-012	3379

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,217	KEETH ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *223-237,247-250 and 466-510* is/are pending in the application.

4a) Of the above claim(s) *466-496* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *233-237, 247-250, 496-510* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the Response filed 08/29/2002. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claim 223 is rejected under 35 U.S.C. 102(e) as being anticipated by Morishita et al (USP 5757175) (newly cited).

As to claim 223, Morishita et al discloses in figures 17 and 19 a voltage reference circuit responsive to an external voltage (ExtVcc) for supplying a reference voltage (INVcc), comprising: an active reference circuit (VGR, figure 19) for receiving the external voltage and for producing a reference signal (Vref) having a desired relationship with the external voltage, the active reference circuit comprising a current source (TP4) utilizing a current mirror for providing current to a diode stack (CVC) having an adjustable impedance; and a unity gain amplifier (CMP, DT) responsive to the reference signal for producing the reference voltage.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 225-227 and 496, 499 and 500 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Furumochi (USP 5473277).

As to claims 225 and 496, Morishita's figure 19 shows the diode stack includes a plurality of transistors (Pra, PRb) connected in series, with each transistor's gate connected to a common potential (ground), and a plurality of fuses (La, Lb) each for shunting one of the transistors. Morishita et al. to shows each of the plurality of switches selectively shunts of the transistors. However, Furumochi's figures 1-6 show a method of using switches for shunting diodes for the purpose of reversibly controlling the output voltage. Furthermore, it is well known in the art that switch transistor having more advantage than fuse because it can be opened and closed selectively. Therefore, it would have been obvious to one having ordinary skill in the art to replace Morishita's fuses with switches for the purpose of reversibly and selectively controlling the output voltage.

As to claims 226 and 499, Furumochi's figures 3 and 5 teaches the switch can be controlled by fuse. Therefore, it would have been obvious to one having ordinary skill in the art to use fuses to control the switches (to turn on or off the switches) based on particular design.

As to claims 227 and 500, Furumochi's figure 5 shows a witch (SWO(TN4)) is made of Field Effect Transistor. Therefore, it would have been obvious to one having ordinary skill in the art to use Field Effect Transistors for the plurality of switches, and Morishita's figure 19 shows the plurality of transistors includes a first plurality of field effect transistors.

3. Claims 228-231 and 501-504 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Park (USP 5448199).

As to claims 228 and 501, Morishita et al's figures 17 and 19 fail to shows a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value. However, Park's figure 3 shows a reference circuit having a pullup stage (100) for pulling up the reference voltage in a burn-in mode to check long term performance of the circuit under condition of high voltage and high temperature. Therefore, it would have been obvious to one having ordinary skill in the art to connect circuit Park's circuit 100, wherein circuit 100 is the "pullup stage", to the output of the Morishita's unity gain amplifier for the purpose to check long term performance of the circuit under condition of high voltage and high temperature in burn-in mode.

As to claims 229 and 502, Park's figure 3 shows the pullup stage includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 230 and 503, from the rejection above, it is inherent that the reference voltage is the external voltage less a voltage drop across the plurality of diodes.

4. Claims 231 and 504 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al (USP 6127881) (newly cited) in view of Morishita et al. (USP 5757175).

As to claims 231 and 504, Tsay's figure 2 shows a multiplier circuit for for generating a voltage signal higher than a reference voltage (Vref). Thus, Tsay's figure 2 shows all limitations of the claims except for detail of the reference circuit. However, Morishita's figures 17 and 19 shows a reference circuit comprising an active reference circuit (VRG) and a unity gain circuit (CMP, DT). Morishita's figure 17 having the advantage of generating a stable reference signal. Therefore, it would have been obvious to one having ordinary skill in the art use Morishita's figure 17 for Tsay's reference circuit for the purpose of having a stable reference signal.

5. Claims 232-233 and 505-506 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) (previous cited) in view Tsay et al (USP 6127881) and of Morishita et al. (USP 5757175).

As to claims 232 and 505, Hayakawa shows in figure 2 a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value and supplying a step down voltage when the external voltage is above the predetermined value. Thus, Hayakawa shows all limitations of the claim except for the detail of the internal stepdown circuit (13). However, the combination of Morishita et al's figure 17 and Tsay et al's figure 2 shows a detail of an internal step down circuit (see the rejection of claim 231). Morishita et al's figure 17 and Tsay et al's figure 2 having an advantage of providing a stable internal signal. Therefore, it would have been obvious to one having ordinary skill in the art to use the combination of Morishita et al's figure 17 and Tsay et al's figure 2 circuit for Hayakawa et al's internal stepdown circuit (13) for the purpose of providing a stable internal signal.

As to claims 233 and 506, Hayakawa et al.'s figure 2 shows the circuit for supplying includes a switch (14) for shorting a bus carrying the external voltage with a bus carrying the output voltage.

6. Claims 234-237, 247-250 and 507-510 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) (previous cited) in view of Tsay et al (USP 6127881) and of Morishita et al. (USP 5757175) and Park (USP 5448199).

The combination above shows all limitations of the claims except for a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value. However, Park's figure 3 shows a

reference circuit having a pullup stage (100) for pulling up the reference voltage in a burn-in mode to check long term performance of the circuit under condition of high voltage and high temperature. Therefore, it would have been obvious to one having ordinary skill in the art to connect circuit Park's circuit 100, wherein circuit 100 is the "pullup stage", to the output of the Morishita's unity gain amplifier for the purpose to check long term performance of the circuit under condition of high voltage and high temperature in burn-in mode.

As to claims 235 and 508, Park's figure 3 shows the pullup stage includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 236 and 509, from the rejection above, it is inherent that the reference voltage is the external voltage less a voltage drop across the plurality of diodes.

As to claims 237 and 510, from the rejection above it is inherent that the combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

Claim 247 recites similar limitations of claims 232-237. Therefore, it is rejected for the same reasons.

As to claim 248, Morishita et al.'s figure 19 shows the step generating a current (I) related to external voltage, apply a current to a circuit node (Vref), and draining the current from the circuit node through an adjustable impedance (CVC).

As to claim 249, from the rejection above, it is inherent for the step of adjusting the impedance to modify the reference signal.

As to claim 250, it is inherent for the step of adjusting the impedance includes the step of opening a fuse.

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive. Applicant states that: Morishita does not use "a unity gain amplifier responsive to said reference signal for producing the reference voltage". The examiner respectfully disagrees. It is notorious well known in the art that unity gain amplifier is an amplifier having the gain of one (1) (Vout/Vin = 1). As admitted by the applicant that Morishita states "...This internal power supply down-converter therefore maintains the internal power supply voltage INVcc at the reference voltage Vref level...". Thus, the internal power supply voltage INVcc is equal to the reference voltage Vref level. The gain of circuit (CMP, DT) is INVcc/Vref = 1. Therefore, circuit (CMP, DT) is a unity gain amplifier circuit.

The same reasons for the arguments of claims 224-237, 247-250 and 496-510.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
January 16, 2003

Terry D. Cunningham
Primary Examiner